

CUSTOMER NO.: 24498  
Serial No.: 10/620,738  
Office Action dated: 04/04/06  
Response dated: 06/30/06

PATENT  
PD020078

Amendments to the Claims

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of the Claims

1. (Currently amended) Method for cross interleave Reed-Solomon code correction comprising the steps of:

inputting a first C1 codeword into C1 decoder means from a first memory means;

outputting a second C1 codeword into a second memory means from the C1 decoder means;

de-interleaving the second C1 codeword to produce a first C2 codeword in the second memory means;

inputting the first C2 codeword into C2 decoder means from the second memory means;

outputting of a second C2 codeword into the second memory means from the C2 decoder means,

wherein the second C2 codeword is the corrected first C2 codeword in case the first C2 codeword is correctable, and the second C2 codeword being a copy of the first C2 codeword in case the first C2 codeword is not correctable.

2. (Original) Method according to claim 1, wherein the second C1 codeword being the corrected first C1 codeword, in case the first C1 codeword is correctable and the second C1 codeword being a copy of the first C1 codeword in case the first C1 codeword is not correctable.

3. (Original) Method according to claim 2, wherein an erasure flag is set for each symbol in the second C1 codeword in case the first C1 codeword is not correctable.

**CUSTOMER NO.: 24498**  
**Serial No.: 10/620,738**  
**Office Action dated: 04/04/06**  
**Response dated: 06/30/06**

**PATENT**  
**PD020078**

4. (Canceled).

5. (Canceled).

6. (Currently amended) Method according to claim 51, further comprising setting an erasure flag for each symbol in the second C2 codeword in case the first C2 codeword is not correctable.

7. (Currently amended) Method according to claim 1, further comprising:  
    inputting the second C1 codeword into the C1 decoder means from the second memory means;  
    outputting a third C1 codeword into a third memory means from the C1 decoder means;  
    de-interleaving the third C1 codeword to produce a third C2 codeword in the third memory means.

8. (Original) Method according to claim 7, wherein the third C1 codeword being the corrected second C1 codeword in case the second C1 codeword is correctable, and the third C1 codeword being a copy of the second C1 codeword in case the second C1 codeword being not correctable.

9. (Original) Method according to claim 8, further comprising setting an erasure flag for each symbol in the third C1 codeword in case the second C1 codeword is not correctable.

10. (Original) Method according to claim 7, further comprising:  
    inputting the third C2 codeword into the C2 decoder from the third memory means;  
    outputting a fourth C2 codeword into a fourth memory means from the C2 decoder means.

**CUSTOMER NO.: 24498**  
**Serial No.: 10/620,738**  
**Office Action dated: 04/04/06**  
**Response dated: 06/30/06**

**PATENT**  
**PD020078**

**11. (Original) Method according to claim 10, wherein the fourth C2 codeword being the corrected third C2 codeword in case the third C2 codeword is correctable, and the fourth C2 codeword being a copy of the third C2 codeword in case the third C2 codeword is not correctable.**

**12. (Original) Method according to claim 11, further comprising setting an erasure flag for each symbol in the fourth C2 codeword in case the third C2 codeword is not correctable.**

**13. (Canceled).**

**14. (Canceled).**

**15. (Canceled).**